The opinion in support of the decision being entered today is *not* binding precedent of the Board.

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte CHAD A. COBBLEY and
TIMOTHY L. JACKSON

Appeal 2007-1772
Application 10/672,750
Technology Center 2800

Decided: August 22, 2007

Before CHUNG K. PAK, PETER F. KRATZ, and
JEFFREY T. SMITH, *Administrative Patent Judges*.

KRATZ, *Administrative Patent Judge*.

DECISION ON APPEAL

This is a decision on an appeal from the Examiner's final rejection of claims 35, 37-39, 45, 47-49, 63, 65-70, the only claims that remain pending in this application. We have jurisdiction pursuant to 35 U.S.C. §§ 6 and 134.

Appellants' invention is directed to an integrated circuit comprising a die stack coupled to a substrate. Claims 35, 45, 48, 68, and 70 are illustrative and reproduced below:

35. An integrated circuit comprising:

a stack comprising at least two semiconductor die, each of the semiconductor die being coupled together by a first adhesive, the first adhesive being curable at a first temperature; and

a substrate coupled to one of the at least two semiconductor die by a second adhesive, the second adhesive being curable at a second temperature lower than the first temperature;

wherein each die in the stack of at least two semiconductor die is electrically functional.

45. An integrated circuit comprising a stack of at least two semiconductor die, each of the die being coupled to an adjacent die in the stack by a respective layer of adhesive prior to the stack being coupled to a packaging substrate, wherein each die in the stack of at least two semiconductor die is electrically functional.

48. An integrated circuit comprising a stack of at least two semiconductor die, each of the die being coupled to an adjacent die in the stack by a respective layer of adhesive prior to the stack being coupled to a packaging substrate, wherein the stack of at least two semiconductor die is configured such that the stack comprises a shingle stack.

68. An integrated circuit comprising:

a stack comprising at least two semiconductor die, each of the semiconductor die being coupled together by a first adhesive, the first adhesive being curable at a first temperature; and

a substrate coupled to one of the at least two semiconductor die by a second adhesive, the second adhesive being curable at a second temperature lower than the first temperature;

wherein each die in the stack of at least two die is successively thinner than the previous die.

70. An integrate circuit package comprising:

a substrate; and

a die stack coupled to the substrate, wherein the die stack comprises at least two semiconductor die coupled together and wherein the die stack is formed prior to being coupled to the substrate;

wherein each die in the stack is successively thinner than the previous die.

The Examiner relies on the following prior art references as evidence in rejecting the appealed claims:

Pai	US 6,503,776 B2	Jan. 7, 2003
Hakey	US 6,627,477 B1	Sep. 30, 2003
Huang	US 6,753,206 B2	Jun. 22, 2004

Claims 35, 37-39, 45, 47-49, 63, and 65-67 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Pai in view of Huang. Claims 68-70 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Pai in view of Hakey.

We affirm the Examiner's rejection of claims 45, 47-49, 63, 65-67, 69 and 70. We reverse the Examiner's rejection of claims 35, 37-39, and 68. Our reasoning follows:

Rejection over Pai in view of Huang

Claims 45, 47-49, 63, and 65-67

The integrated circuit of claims 45 and 47-49 requires a die stack of at least two semiconductor die. The semiconductor die are coupled to each other by an adhesive layer and the stack of die are coupled to a packaging substrate. In addition, independent claim 45 requires that each die is electrically functional whereas independent claims 48 and 66 require the die to be stacked in a shingle stack arrangement.[1] Like claim 45, independent claim 63 and dependent claim 65 require the die to be electrically functional but do not require the use of an adhesive layer or a shingle stack arrangement in coupling the die.

Respecting rejected claims 45, 47-49, 63, and 65-67, Appellants contend that Pai, taken alone or in combination with Huang, does not disclose or suggest a die stack wherein each die is electrically functional and/or the die are stacked in a shingle stack arrangement as variously recited in these claims.

Thus, the principal issue before us with respect the Examiner's obviousness rejection of claims 45, 47-49, 63, and 65-67 is: Have Appellants identified reversible error in the Examiner's § 103(a) rejection of any of claims 45, 47-49, 63 and 65-67 by the assertion that the applied references would not have taught or suggested a die stack arrangement wherein each die is electrically functional and/or the die are shingle stacked? We answer the question in the negative and affirm the Examiner's rejection of claims 45, 47-49, 63, and 65-67 for reasons set forth by the Examiner in the Answer and as further explained below.

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[1] Appellants explain that die "shingle stacks" are die stacks wherein an edge of a stacked die overhangs the edge of another die of the stack (Specification p. 14, l. 9 - p. 15, l. 6).

Under 35 U.S.C. § 103, the factual inquiry into obviousness requires a determination of: (1) the scope and content of the prior art; (2) the differences between the claimed subject matter and the prior art; (3) the level of ordinary skill in the art; and (4) any secondary considerations. *Graham v. John Deere Co. of Kansas City*, 383 U.S. 1, 17-18, 148 USPQ 459, 467(1966). "[A]nalysis [of whether the subject matter of a claim would have been obvious] need not seek out precise teachings directed to the specific subject matter of the challenged claim, for a court can take account of the inferences and creative steps that a person of ordinary skill in the art would employ." *KSR Int'l v. Teleflex, Inc.*, 127 S. Ct. 1727, 1740-41, 82 USPQ2d 1385, 1396 (2007); *see also DyStar Textilfarben GmBH & Co. Deutschland KG v. C.H. Patrick Co.*, 464 F.3d 1356, 1361, 80 USPQ2d 1641, 1645 (Fed. Cir. 2006) ("The motivation need not be found in the references sought to be combined, but may be found in any number of sources, including common knowledge, the prior art as a whole, or the nature of the problem itself."); *In re Bozek*, 416 F.2d 1385, 1390, 163 USPQ 545, 549 (CCPA 1969) ("Having established that this knowledge was in the art, the examiner could then properly rely, as put forth by the solicitor, on a conclusion of obviousness 'from common knowledge and common sense of the person of ordinary skill in the art without any specific hint or suggestion in a particular reference.'"). The analysis supporting obviousness, however, should be made explicit and should "identify a reason that would have prompted a person of ordinary skill in the art to combine the elements" in the manner claimed. *KSR*, 127 S. Ct. at 1731, 81 USPQ2d at 1389.

Here, Appellants do not dispute that Pai discloses or suggests an integrated circuit including at least two semiconductor die arranged in a

stack and coupled to a packaging substrate. *See* the Brief and the Reply Brief in their entirety, and Pai, col. 1, ll. 5 - 63 and col. 2, l. 15 - col. 3, l. 56. Rather, Appellants argue that Pai, alone or in combination with Huang, does not disclose or suggest that each die in the stack in electrically functional, as claimed (*see*, e.g., appealed claims 45, 47-49, 63, 65 and 67) and/or that the die are not taught or suggested as being shingle stacked (*see* claims 48 and 66).

Regarding the claimed "electrically functional" feature, we give this disputed claim term the broadest reasonable construction consistent with Appellants' Specification as it would be understood by one of ordinary skill in the art. In proceedings before the PTO, claims in an application are to be given their broadest reasonable interpretation consistent with the Specification, and the claim language should be read in light of the Specification as it would be interpreted by one of ordinary skill in the art. *In re Sneed*, 710 F.2d 1544, 1548, 218 USPQ 385, 388 (Fed. Cir. 1983). Moreover, limitations are not to be read into the claims from the Specification. *In re Van Geuns*, 988 F.2d 1181, 1184, 26 USPQ2d 1057, 1059 (Fed. Cir. 1993) citing *In re Zletz*, 893 F.2d 319, 321, 13 USPQ2d 1320, 1322 (Fed. Cir. 1989).

Applying these principles to the disputed claim term, "electrically functional," we agree with the Examiner that this term is not defined in Appellants' Specification and is encompassing of any electrical functionality, including an insulation, spacing or other auxiliary electrically related function with respect to the integrated circuit package being claimed. We note, for example, that Appellants did not limit these appealed claims to require that all of the die in the stack are electrically coupled to the substrate

via bond wires or by other connective devices to serve any particular electrical function as part of the integrated circuit package. Given this claim construction, we agree with the Examiner that Appellants' arguments against the Examiner's rejection of claims 45, 47-49, 63, 65 and 67 on the basis that the stack of Pai includes a non-electrically functional die (*see*, e.g., die 160, Fig. 8) is unpersuasive of any reversible error in the Examiner's obviousness rejection.

In any event, we note that Pai discloses that it is known to employ adhesive without a dummy die to space die that are connected via bondwire to a substrate (Pai, col. 1, ll. 33-62 and drawing Fig. 1. Thus, even if we agreed with Appellants' interpretation of the claim term "electrically functional", which we do not, Pai teaches/suggests the option of forming stacks, wherein all of the chips (die) are electrically functional in a manner within the meaning of Appellants' argued more limited definition for that claim term.[2]

Appellants' argue that eliminating a dummy die in the disclosed inventive integrated circuit package of Pai would change the principle of operation of the Pai device (Br. 18). We are not persuaded by this argument.

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[2] We have determined that the teachings of Pai, by itself, are sufficient to render the formation of a stack with all of the chips/die thereof being electrically functional, as claimed. Thus, we need not further discuss the additional teachings of Huang, as referred to by the Examiner as an option, in further support of showing that this claimed feature (all stacked die being electrically functional) would have been obvious to one of ordinary skill in the art at the time of the invention.

In this regard, one of ordinary skill in the art would clearly grasp that the so-called "dummy die" of Pai are merely substitutes/additions to the adhesive bonds formed between electrically connected stacked die of a packaged device, as disclosed in the Background portion of the disclosure of Pai. While Pai may disclose that prior art dummy die –free packages are assembled with some difficulty, Pai does not teach that eliminating a dummy die would render the integrated circuit package device inoperative or substantially alter the function or mode of operation thereof.

Appellants argue that the applied prior art does not teach or suggest a shingle stack arrangement for the stacked die as called for in claims 48 and 66 (Br. 20). However, the artisan is presumed to have some capability in combining the die into a stack form. "The combination of familiar elements according to known methods is likely to be obvious when it does no more than yield predictable results." *KSR Int'l v. Teleflex Inc.*, 127 S. Ct. at 1739, 82 USPQ2d at 1395. The question to be asked is "whether the improvement is more than the predictable use of prior art elements according to their established functions." *Id.*

Stacked chip packages, which are the subject matter of Pai's U.S. Patent and Appellants' Specification and Claims, are clearly known by one of ordinary skill in the art as an integrated circuit package arrangement that allows chip combinations in an integrated circuit package, while saving space as evidenced by a review of the "Background of the Invention" Section of Pai's disclosure. Compare Appellants' "Description of the Related Art" (Specification 1-4). The question before us with respect to Appellants' claimed "shingle stack" arrangement is: Would one of ordinary skill in the art have recognized that chips or die, to be stacked, may come in

different sizes such that the use of an overhang or offset (shingle stack) stacking arrangement would have been a recognized obvious option to one of ordinary skill in the art in forming the stacked die product of Pai? We answer this question in the affirmative.

We recognize that Huang is directed to a dual-chip integrated circuit package wherein the chips are located on opposing sides of a metal leadframe substrate (*see*, e.g., Huang, Fig. 2, Fig. 10) whereas here the claimed integrated circuit stacks, as well as Pai's stacks involve chips (die) that are stacked together on the same side of a substrate. Nonetheless, Huang clearly evinces that packageable integrated circuit chips come in different sizes and are designed for different purposes or functions that can be used in combination in an integrated circuit (col. 2, ll. 12-15 and 44-47).

From the combined teachings of these references, one of ordinary skill in the art would have recognized the obviousness of using the stacking arrangement of Pai for stacking chips (die) of differing sizes, including chips having differing diameters such that an overhang or "shingle stack" stacking arrangement would have commended itself as an available option to an ordinarily skilled artisan faced with the task of stacking die of differing sizes for forming integrated circuit packages. Indeed, Appellants acknowledge a considerable skill level is expected of one of ordinary skill in this art (Specification 5: ll. 8-17).

In light of the above and for reasons as set forth in the Answer, Appellants' arguments concerning the combinability of Pai and Huang for teaching/suggesting the overhang of dies stacked in an integrated circuit package are not persuasive (Br. 19-20; Reply Br. 6). In this regard, we note that the test for obviousness is not whether the features of a secondary

reference may be bodily incorporated into the structure of the primary reference. . . . Rather, the test is what the combined teachings of those references would have suggested to those of ordinary skill in the art. *In re Keller*, 642 F.2d 413, 425, 208 USPQ 871, 881 (CCPA 1981). *See also In re Sneed*, 710 F.2d 1544, 1550, 218 USPQ 385, 389 (Fed. Cir. 1983) ("[I]t is not necessary that the inventions of the references be physically combinable to render obvious the invention under review."); and *In re Nievelt*, 482 F.2d 965, 968, 179 USPQ 224, 226 (CCPA 1973) ("Combining the teachings of references does not involve an ability to combine their specific structures.").

It follows that, on this record, we shall affirm the Examiner's obviousness rejection of claims 45, 47-49, 63, and 65-67 over Pai in view of Huang.

Our disposition of the Examiners rejection of claims 35 and 37-39 over Pai in view of Huang is another matter. This is because all of these claims require that the substrate is coupled to one of the semiconductor die by an adhesive different from the adhesive coupling the semi-conductor die to each other. The substrate coupling adhesive is required to be curable at a temperature that is lower than the cure temperature of an adhesive that is used for coupling the semiconductor die together. The Examiner maintains that this argued claim feature respecting the different adhesives relates to a product-by–process limitation that is given no patentable weight. (Answer 4-5). However, this claim feature relates to a property of the adhesives used in the claimed product, not just a method of making the product. The Examiner has not otherwise furnished a rationale explanation for the proposed rejection of the claims requiring this feature. In this regard, the

portion of the disclosure of Pai referred to by the Examiner (Answer 21) does not address the characteristics of the adhesive used by Pai for coupling the substrate to a semi-conductor die as correctly argued by Appellants (Reply Br. 6-7). In short, the Examiner's rationale for the rejection does not "identify a reason that would have prompted a person of ordinary skill in the art to combine the elements" in the manner claimed. *KSR Int'l v. Teleflex, Inc.*, 127 S. Ct. at 1731, 82 USPQ2d at 1389).

On this record, we reverse the Examiner's § 103(a) rejection of claims 35 and 37-39 over the combined teachings of Pai and Huang.

Rejection over Pai in view of Hakey

Claim 68

Claim 68 requires an integrated circuit comprising a die stack wherein the substrate is coupled to one of the semi-conductor die using an adhesive that is curable at a lower temperature than the curing temperature of an adhesive used in coupling the semiconductor die together.

Here, the Examiner makes the same reversible error in not giving the adhesive properties of the claimed product patentable weight and by referring to a portion of Pai that is directed to an adhesive other than the substrate coupling adhesive, as we discussed above with respect to the Examiner's rejection of claims 35 and 37-39 (*see* Answer 11 and 22). The Examiner has not explained how the teachings of Hakey would remedy this deficiency in the stated rejection. It follows that we shall reverse the Examiner's § 103(a) rejection of claim 68 over Pai in view of Hakey.

Claims 69 and 70

Appealed claims 69 and 70 do not require the adhesive properties discussed above with respect to claim 68. Rather, claims 69 and 70 require

the at least two die in the stack to be successively thinner. In other words, for a two die stack, the die are required to have thicknesses that differ from one another; that is, the thicknesses of each die of a two die stack are not identical.

As explained by the Examiner (Answer 13), Pai teaches that it is known to combine chips having differing functions, such as processor, memory, and logic chips in a single package (Pai, col. 1, ll. 13-20). The Examiner additionally refers to Hakey to evidence that semiconductor chips that are used together in a package are known to have differing sizes, including thicknesses (Hakey, col. 2, ll. 31-40). Based, on those disclosures, the Examiner has reasonably found that, while Pai does not expressly teach that the chips combined in a stack have identical or non-identical thicknesses, it would have been obvious to one of ordinary skill in the art to stack die of differing thicknesses in the package of Pai.

Appellants maintain that Hakey arranges chips in a co-planar fashion rather than stacking the chips. Hence, Appellants assert that Hakey teaches away from 'ppellants' claimed stacking arrangement such that it would not have been obvious to one of ordinary skill in the art to combine the teachings of Pai and Hakey (Br. 26).

Have Appellants identified reversible error in the Examiner's obviousness rejection of claims 69 and 70 by the asserted "teaching away" contention presented in the Brief? We answer this question in the negative and affirm the Examiner's § 103(a) rejection of claims 69 and 70.

As to the specific question of "teaching away," our reviewing court in *In re Gurley*, 27 F.3d 551, 553, 31 USPQ2d 1130, 1131 (Fed. Cir. 1994) stated:

> [a] reference may be said to teach away when a person of ordinary skill, upon [examining] the reference, would be discouraged from following the path set out in the reference, or would be led in a direction divergent from the path that was taken by the applicant.

Here, the Examiner relies on Hakey for showing that it is well known in the art that die come in different thicknesses. Hakey's disclosure of a non-stacked die packaging arrangement does not rise to the level of a general teaching away from the use of stacked die, especially given the known use of such an alternative packaging arrangement as taught by Pai. Rather, one of ordinary skill in the art faced with the desire to conserve space would have been led to consider the available option of stacking the die, whether the die are of the same or differing thicknesses based on the combined teachings of the references. The fact that non-stacked die packaging options are available does not serve to detract from the Pai teaching/suggestion of using stacked die packages.

It follows that, on this record, we shall affirm the Examiner's § 103(a) rejection of claims 69 and 70 over Pai in view of Hakey.

CONCLUSION

The decision of the Examiner to reject claims 45, 47-49, 63, 65-67 under 35 U.S.C. § 103(a) as being unpatentable over Pai in view of Huang; and to reject claim 68 under 35 U.S.C. § 103(a) as being unpatentable over Pai in view of Hakey is affirmed. The decision of the Examiner to reject claims 35, 37-39 under 35 U.S.C. § 103(a) as being unpatentable over Pai in view of Huang; and to reject claims 69 and 70 under 35 U.S.C. § 103(a) as being unpatentable over Pai in view of Hakey is reversed.

No time period for taking any subsequent action in connection with this appeal may be extended under 37 C.F.R. § 1.136(a)(1)(iv) (2006).

AFFIRMED-IN-PART

tf/ls

Fletcher Yoder (Micron Technology, Inc.)
P.O. Box 692289
Houston, TX 77269-2289